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IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

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| Applicant(s): | Mark I. Gardner, Robert Dawson, H. Jim Fulford, Jr., Frederick N. Hause, Mark W. Michael, Bradley T. Moore, Derick J. Wristers |
| Assignee: | Advanced Micro Devices, Inc. |
| Title: | Dopant Diffusion-Retarding Barrier Region Formed Within Polysilicon Gate Layer |
| Serial No.: | 09/177,047 |
| Filing Date: | October 22, 1998 |
| Examiner: | A. Ghyka |
| Group Art Unit: | 2812 |
| Docket No.: | M-4692 US |
| Client Ref. No.: | TT1618 |





San Jose, California
December 20, 2000

BOX CPA TO 3600 MAIL ROOM
COMMISSIONER FOR PATENTS
Washington, D. C. 20231

**INFORMATION DISCLOSURE STATEMENT**
**UNDER 37 CFR § 1.97(b)**

Dear Sir:

Pursuant to 37 C.F.R. § 1.56, § 1.97 and § 1.98, the documents listed on the accompanying PTO Form-1449 are called to the attention of the Examiner for the above patent application. Copies of these documents are enclosed.

Citation of these documents shall not be construed as:

1. an admission that the documents are necessarily prior art with respect to the instant invention;
2. a representation that a search has been made, other than as described above; or
3. an admission that the information cited herein is, or is considered to be, material to patentability as defined in § 1.56(b).

EXPRESS MAIL LABEL NO:

EL708268675US

Respectfully submitted,

David G. Dolezal
Attorney for Applicant(s)
Reg. No. 41,711

| U.S. Department of Commerce, Patent and Trademark Office | Atty Docket No. | Serial No. |
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| | M-4692 US | 09/177,043 |
| INFORMATION DISCLOSURE STATEMENT BY APPLICANT | Applicant(s) | |
| (Use several sheets if necessary) | Mark I. Gardner, et al. | |
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*EXAMINER: Initial if reference considered, whether or not citation is in conformance with MPEP 609; Draw line through citation if not in conformance and not considered. Include copy of this form with your communication to applicant.

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| | AQ | E. Hasegawa et al., "The Impact of Nitrogen Profile Engineering On Ultra-Thin Nitrided Oxide Films for Dual-Gate CMOS ULSI," *International Electron Devices Meeting Technical Digest*, December 10-13, 1995, Washington, DC, pages 327-330. |
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| | AR | C.T. Liu et al, "25 Å Gate Oxide without Boron Penetration for 0.25 and 0.3-μm PMOSFETs," *1996 Symposium on VLSI Technology Digest of Technical Papers*, pages 18-19. |
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